WHAT IS CLAIMED IS:

1. A semiconductor characteristic evaluation apparatus comprising:

a plurality of measurement units arranged on a chip, on which a plurality of measured patterns of components configuring a semiconductor integrated circuit and varying in kind from component to component are mounted;

a measurement bus group arranged above the plurality of measurement units and connected to the plurality of measured patterns to configure a measurement circuit system in accordance with measured items of the components;

a plurality of measurement pads, on the chip, which are arranged in a region other than an arrangement region of the plurality of measurement units and to which a measuring device is connected;

a plurality of selection switches which select, in accordance with the measured items of the components, a measurement bus group configuring the measurement circuit system in accordance with the measured items and which connect the group to the plurality of measurement pads; and

a control circuit which electrically controls switching of the plurality of selection switches in accordance with the measured items of the components.

2. The semiconductor characteristic evaluation

apparatus according to claim 1, wherein each component configuring the semiconductor integrated circuit is a semiconductor element or an integrated circuit including a semiconductor element, and the plurality of measured patterns are formed by a plurality of semiconductor elements or a plurality of integrated circuits different from one another in structure, size and shape.

3. The semiconductor characteristic evaluation apparatus according to claim 1, wherein one of the components configuring the semiconductor integrated circuit is a delay circuit, and the plurality of measured patterns are formed by a plurality of delay circuits different from one another in delay time.

4. The semiconductor characteristic evaluation apparatus according to claim 1, wherein several tens or several hundreds of kinds of measured patterns are mounted on each of the plurality of measurement units.

5. The semiconductor characteristic evaluation apparatus according to claim 1, wherein each of the plurality of measurement units comprises a plurality of areas in which the plurality of measured patterns are mounted for each component.

6. The semiconductor characteristic evaluation apparatus according to claim 1, wherein the measurement bus group has a first bus arranged in a stripe shape and a second bus arranged in a mesh shape.

7. The semiconductor characteristic evaluation apparatus according to claim 6, wherein for the second bus, a vertical bus and a lateral bus are interconnected to be fixed at equal potentials.

8. The semiconductor characteristic evaluation apparatus according to claim 7, wherein the second bus is divided into a plurality of groups.

9. The semiconductor characteristic evaluation apparatus according to claim 1, wherein the control circuit is arranged on an outer peripheral part of the chip.

10. The semiconductor characteristic evaluation apparatus according to claim 1, wherein one of the components configuring the semiconductor integrated circuit is a metal oxide semiconductor (MOS) transistor; sources and drains of all the transistors among the plurality of measured patterns formed by a plurality of integrated circuits including the MOS transistors are directly connected to the second bus of the measurement bus group arranged in the mesh shape; a gate of a selected transistor is connected through a switch circuit to the second bus allocated for gate bias application; and a gate of an unselected transistor is connected through the switch circuit to the second bus allocated for an off-bias application in which a potential is independently controlled from the outside of the chip.

11. The semiconductor characteristic evaluation apparatus according to claim 1, wherein one of the components configuring the semiconductor integrated circuit is a capacity; for the plurality of measured patterns formed by the plurality of integrated circuits including the capacity, a driving clock signal is supplied through the first bus of the measurement bus group arranged in the stripe shape; and a measurement current obtained by capacity-current conversion is outputted through the first bus of the measurement bus group arranged in the stripe shape.

12. The semiconductor characteristic evaluation apparatus according to claim 11, wherein the first bus through which the driving clock signal is supplied is configured by using a low capacity wiring where a parasitic capacitance is reduced to 0.1 pF/mm; and the first bus through which the measurement current is outputted is configured by using a low capacity and low resistance wiring where a parasitic capacitance is reduced to 0.12 pF/mm and wiring resistance is reduced to 500 Ω/mm.

13. The semiconductor characteristic evaluation apparatus according to claim 11, wherein a selection circuit common to each measurement unit is inserted between the plurality of measured patterns formed by the plurality of integrated circuits and the first bus through which the measurement current is outputted.

14. The semiconductor characteristic evaluation apparatus according to claim 13, wherein the selection circuit is configured by a p-type metal oxide semiconductor (MOS) transistor; a well and a source of the p-type MOS transistor are connected to each other; and a well and a source of each p-type MOS transistor are connected to each other in the plurality of measured patterns to which the p-type MOS transistor is connected.

15. The semiconductor characteristic evaluation apparatus according to claim 5, wherein in the plurality of measurement units, a part of the plurality of areas is shared by setting n (n>1) measurement units as a unit.